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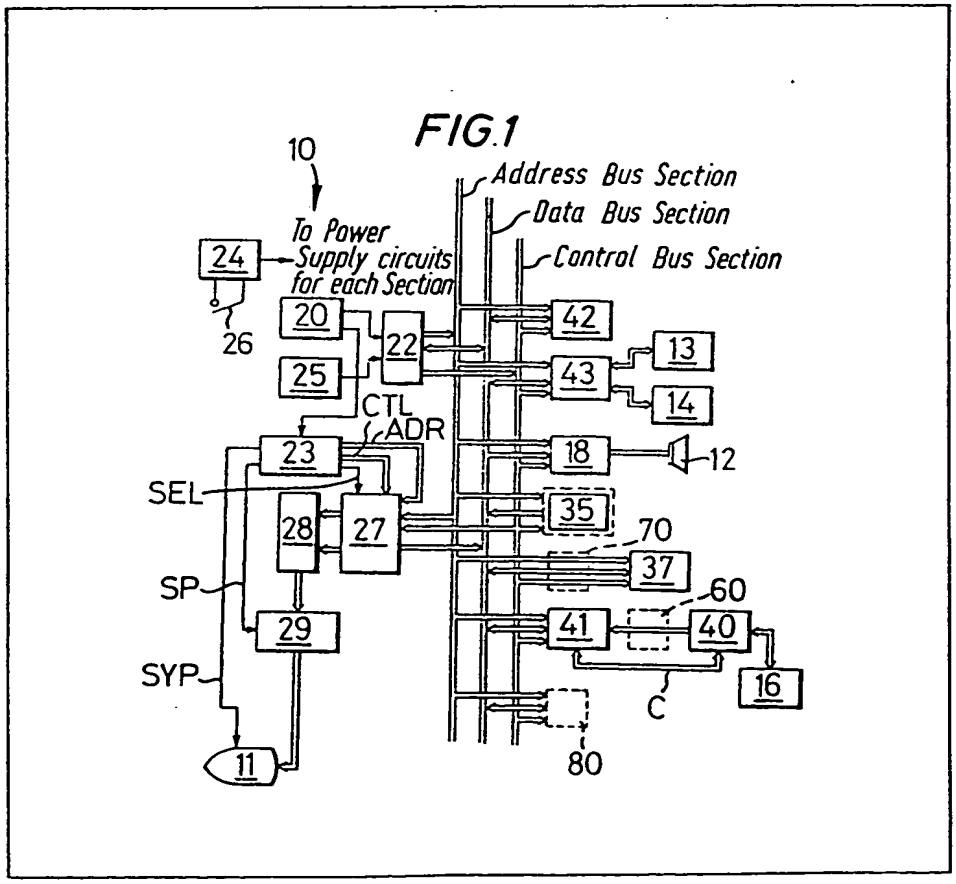
(54) **Video game machine**

(57) A video game machine (10) for electronically displaying a game content on a screen of a video monitor (11) includes a microprocessor (22) for controlling transfer of information relating to a game program from an operating memory (16) to a program memory (37) the operating memory (16) being adapted to be interchangeable with other operating memory or memories, eg tape cassettes or semi-conductor memories.



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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

FIG.1

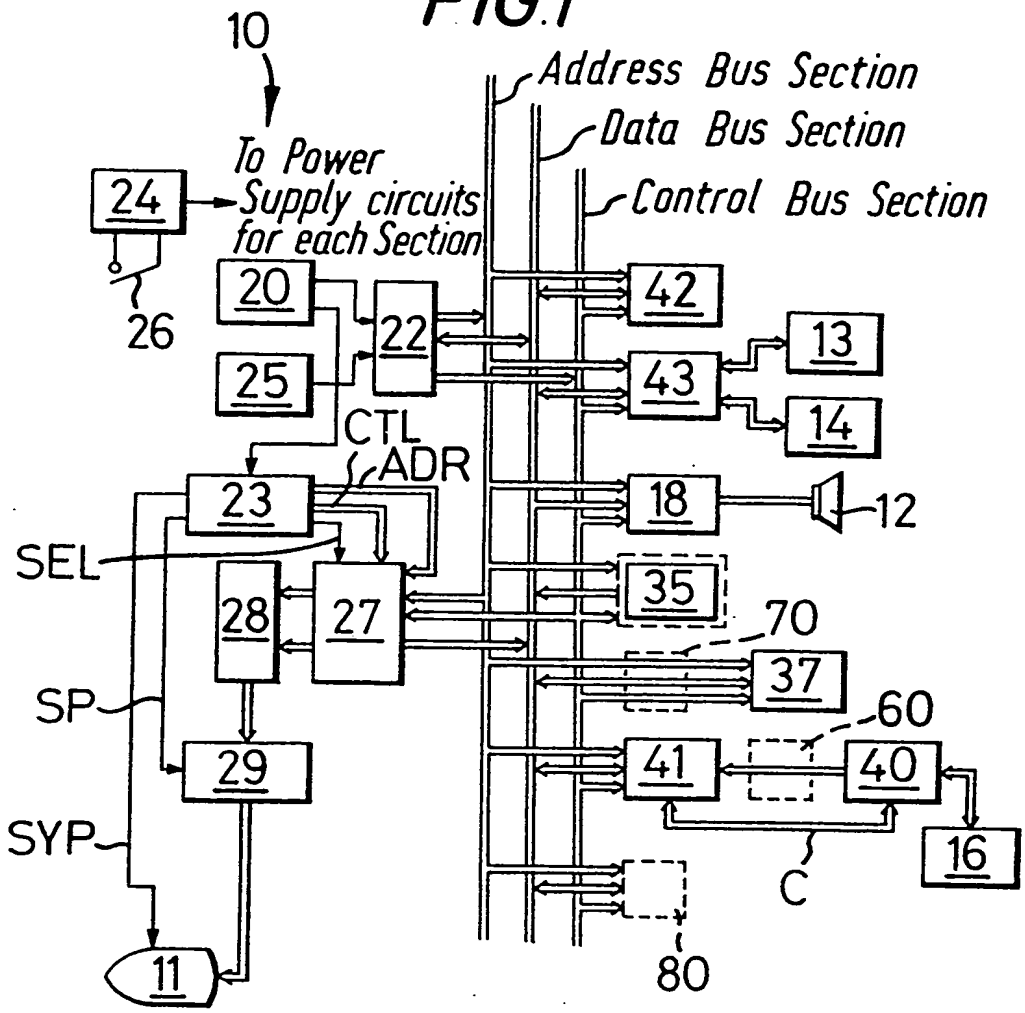

10
To Power
Supply circuits
for each Section
Address Bus Section
Data Bus Section
Control Bus Section
24
26
20
25
22
42
43
13
14
CTL
ADR
23
18
12
SEL
28
27
35
70
37
SP
60
29
41
40
16
SYP
C
11
80

FIG.2

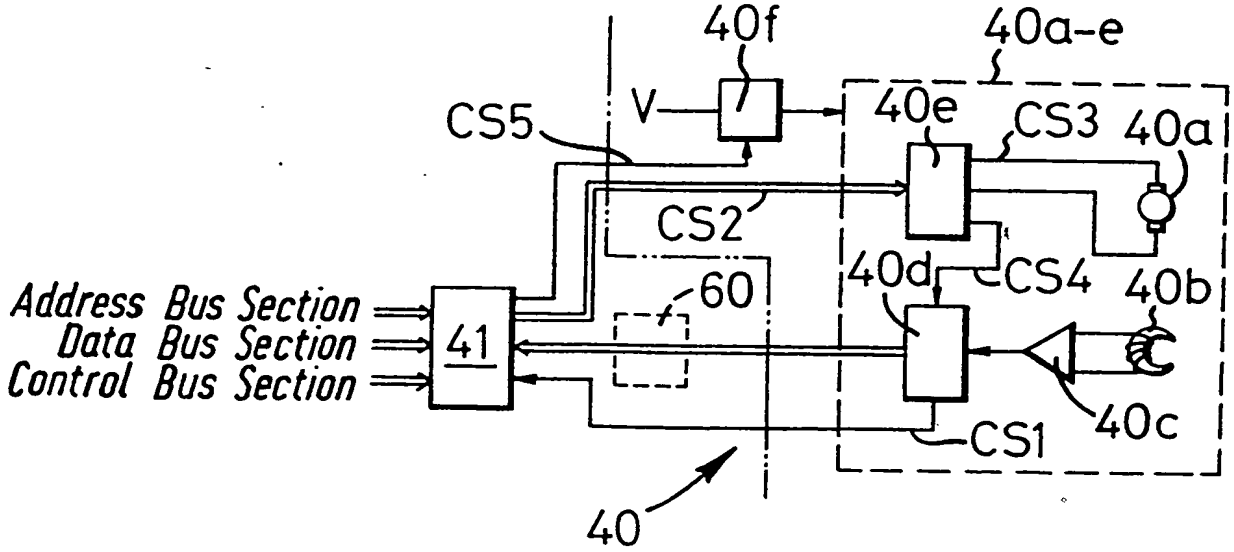

40f
40a-e
V
CS5
40e
CS3
40a
CS2
40d
CS4
40b
Address Bus Section
Data Bus Section
Control Bus Section
60
41
40c
CS1
40

FIG.3

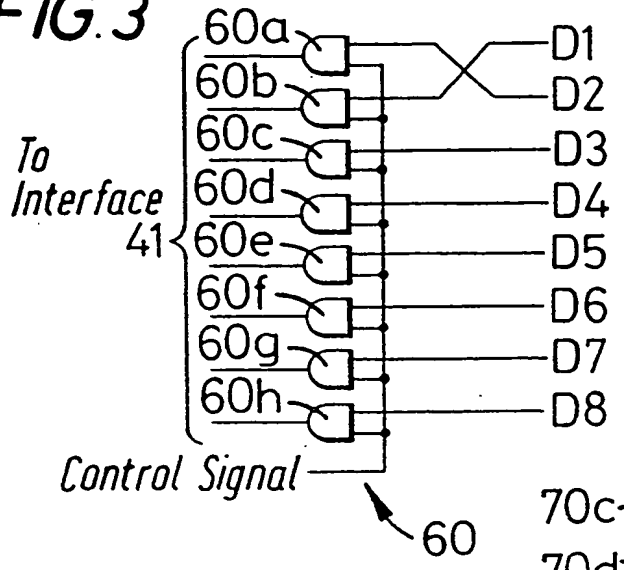


FIG.4

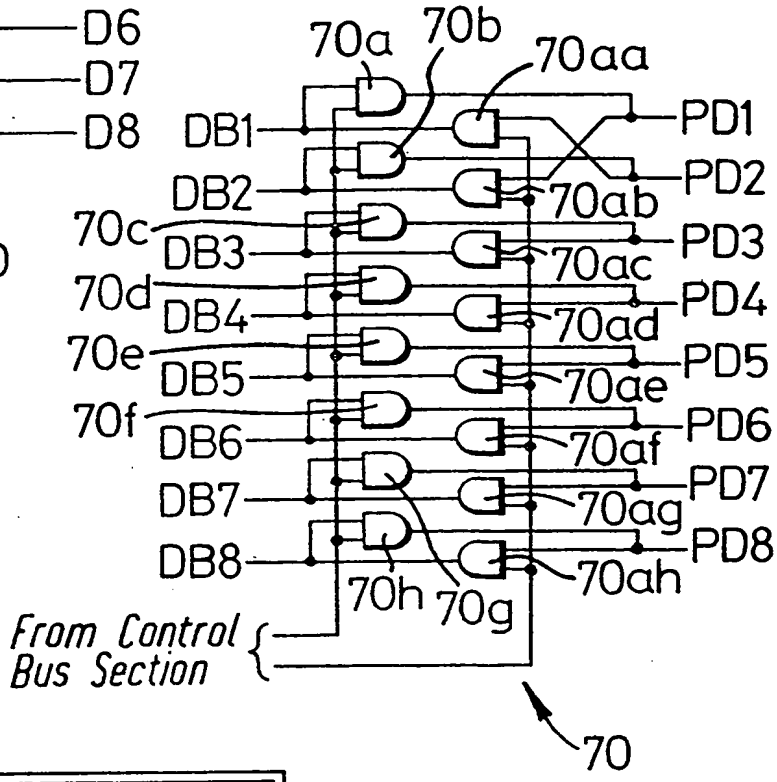
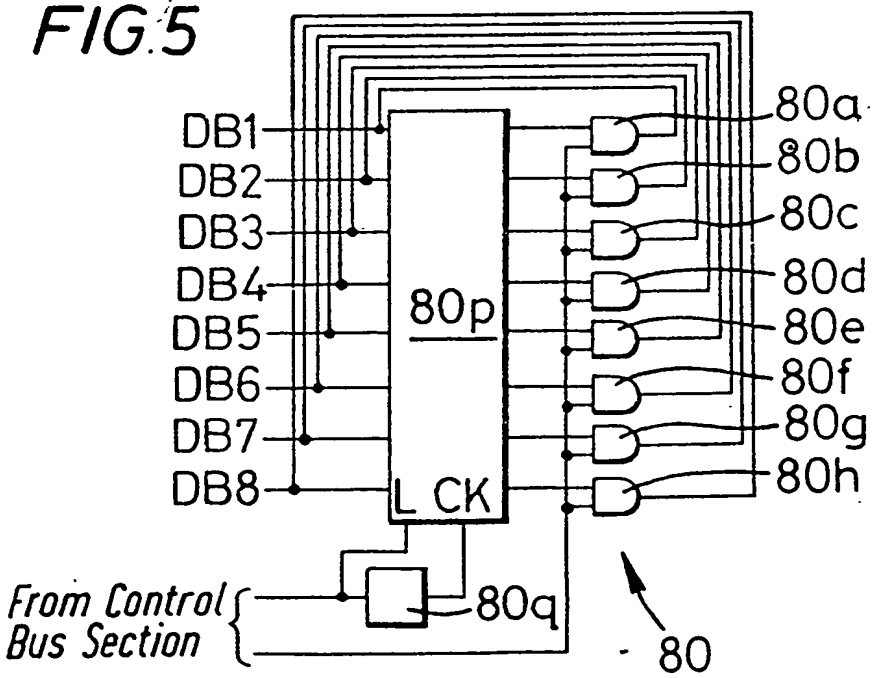


FIG.5



SPECIFICATION

Video game machine

The present invention relates to an improvement in the video or television game machine for electronically displaying a game content to be played with upon a monitor screen.

In reflection of the electronics era, the video games have rapidly come into wide use in many countries of the world. However, because of rather fixed game contents for play, thus resulting in only a limited range of play patterns to be displayed in the machine, it is the general trend that the life cycle of such game machine is turned out to be considerably short, which would inevitably add undue competitions and economical damages in the relevant trade field. As a countermeasure to cope with such uneconomical problems, the traders concerned are obliged to replace obsolete game programs with newly designed ones by way of physical means as necessary, however, there are many possibilities such that the game programs per se may be duplicated or appropriated improperly by a third party, thus resulting in unavoidable undue competitions and hampered order in the circulation in the field concerned.

In this respect, essentially wanted is the advent of an improved video game machine which readily allows new game programs to be inserted or implemented or the total game to be replaced with novelty one by way of electronic scheme.

This invention is essentially directed to the provision of an improved video game machine of construction adapted to electronically display a game content upon a video monitor screen.

According to this invention, there is provided an improved video game machine which is constructed in such a manner that a game player may supply an internal memory with a new game program at any time so desired, and that a microprocessor may read out a new program provided externally of the game machine, when a reset output is received by that microprocessor.

On the other hand, this video game machine is also constructed such that there are provided a circuit with a plurality of interchangeable logic elements adapted to connect to an external memory which can be replaced interchangeabley, so that the above mentioned external program per se is therefore not incorporated in that circuit.

Figure 1 is a block diagram showing the circuit incorporated in the video game machine according to this invention;

Figure 2 is a block diagram showing the control for an external memory shown in Figure 1; and

Figure 3 through *5* are circuit diagrams showing typical several embodiments of this invention wherein a plurality of control logic elements are added to the machine circuit.

The present invention will now be described in detail by way of typical embodiments thereof in conjunction with the accompanying drawings.

Referring to Figure 1, there is shown a block diagram of the video game machine 10 according to this invention by way of a preferred embodiment which comprises an external memory 16 which can be disc nnected by a player, a control 40 for this memory 16, a video monitor 11, a speaker 12, and operating handles 13, 14.

In the first place, the general construction of a display circuit for the above mentioned monitor 11 will now be explained in brief.

In Figure 1, there is shown a microprocessor (CPU) 22 which is adapted to control the whole function of the game machine 10. The output from a pulse generator 20 serves as a timing clock signal for a CPU 22 mentioned above, and as a standard signal for a timing signal generator 23 for a given game pattern.

The timing signal generator 23 stated above is adapted to divide the frequency of a signal from the pulse generator 20, send a signal ADR addressing a video memory 28 while generating a horizontal or vertical timing signal for the monitor screen, and deliver a control signal CTL to a mulitplexer 27 shown in Figure 1 at a different timing.

In the ordinary construction, above mentioned memory 28 comprises a memory which can correspond to the mentioned horizontal/vertical signals, e.g., each of 256 segments. The multiplexer 27 operates to read out the signals at the video memory 28, and switches through a switching signal SEL the above mentioned signal CTL and a signal to be sent through an address bus section and a control bus section, and further through a CPU 22 or a data bus section at the video memory 28.

On the other hand, since a pulse signal from the reset circuit 25 is transmitted to a CPU 22 and to the other resistances, they may be reset, accordingly.

Next, when the address of the video memory 28 is addressed by the above mentioned signal ADR, such address data is converted sequentially to serial signals at a parallel serial conversion circuit 29 which receives the address data.

As the output of such conduit 29 is supplied to the monitor 11, the monitor 11 will operate to scan in accordance with the synchronization signal SYP delivered from the timing signal generator 23, and display thus-obtained game content upon its screen.

The above mentioned monitor 11 functions to electronically display a current game content, as well as a current progress of the game and a current score gained, while the speaker 12 operates in synchronization with the monitor 11. As generally known in conventional video game machine construction, operating handles 13, 14 are arranged to shift vertically and horizontally a beam, a target or targets, and other movable objects in the game display so that a current score play time may be led to be advantageous in a play r's strategy.

According to this invention, there is provided a bootstrap memory 35 which is adapted to store a game program to be read out by an internal memory 37 within the game machine. As a consequence, when operating the external memory 16 comprising a member such as a casette tape, a semiconductor or floppy disc, there starts a then preparation ready to

read out the game program stated ab ve so as to complete such read operation.

In general, the bootstrap memory 35 comprises a P-type ROM, which is the only one that enables the external information to be fed into th program memory 37 as desired.

Next, description will now be given on the construction of the external memory 16 and the control 40 therefore. The memory 16 serves to receive an external information from a CPU 22 or other control circuit through an interface 41, which information is in the form of a multiplicity of blocks and is to be delivered to the program memory 37.

The control 40 for the external memory is operatively connected with a drive motor (see Figure 1) so as to transfer such external information under the control into the game machine. For example, this control operates to control the running and stopping of a casette tape as the external memory 16 so that it may read out a data block by block from this tape. If the external memory 16 is of a semi-conductor member, this control will provide an appropriate bias so as to read sequentially the game content stored therein.

In the case stated above, a working memory 42 shown in Figure 1 operates to temporarily store data during the operation of a CPU 22, while a panel interface 43 functions to direct the signals from the operating handles 13, 14 to a CPU 22, accordingly.

Now, Figure 2 shows, in a block diagram form, the general construction of the control 40 for use with a casette tape as the external memory 16 as stated above. More specifically, the above mentioned control 40 comprises a drive motor 40*a*, a magnetic head 40*b* for reading an external information, a head output amplifier 40*c* and an external information converter 40*d*. This control is adapted to convert the information read by the head 40*b* to be serial and parallel, whereupon the information converter 40*d* delivers a control signal CS_1 or other necessary information to a CPU 22.

The above mentioned information converter 40*d* incorporates a circuit adapted to convert the information read by the head 40*b* to be serial and parallel and a counter adapted to generate a control signal (which counts through a decoder 40*e* to deliver a signal CS_4 which can reset thus-obtained count). With such construction, the control 40 sends out a signal CS_3 for controlling the running speed of the drive motor 40a upon the receipt of a signal CS_2 from a CPU 22 (which includes signals for controlling the running and stopping motion of the tape).

With the construction of the control 40 stated above in connection with Figure 2 that there is also provided a gate 40f adapted to be controlled with a signal CS_5 from a CPU 22, the signal CS_5 may be received by this gate 40*f*. Consequently, there is applied a supply voltage V to the circuit comprising 40*a* through 40*e*.

Now with the construction of the video game machine according to this invention as stated above so that each of functions described above may occur in cooperation with each other, it is seen that the object of preventing a possible improper appropriation or duplication of the game program per se is now attained accordingly. Hereinafter, description will now be given on the operation of the invention in brief.

When the video game machine according to this invention is started in operation with the signal CS_5 sent from the CPU 22, the reset circuit 25 will deliver its pulse signal to a CPU 22, upon the receipt of which pulse a CPU 22 now accesses the bootstrap memory 35, the game machine operates initially to set or reset data.

Next, a CPU 22 reads a next program as as to deliver thus-obtained information to the external memory control 40. According to the operation of the control 40 as reviewed herein, it is now prepared to read out the external information received. In case that the external memory 16 is of a casette tape, the memory control 40 sends thus-obtained information through the interface 41 either directly or through a CPU 22 to the internal memory 37.

In this manner, at the moment a CPU 22 senses that the external information necessary for developing a game is read out, the external memory retrieve mode is now shifted and there is set up a game to be started with.

When a player puts a metallic currency or coin into the slot of the game machine, a CPU 22 accesses the multiplexer 27 and the external information stored in the game machine memory is transferred to the video memory 28, the mentioned information thus-fed by way of the address signal and control signal being sent to the paralle-serial conversion circuit 29. Then, the output from the circuit 29 is fed to the video monitor 11 so as to display a video game background and movable elements on the monitor screen, accordingly.

Now, the means for preventing improper appropriation and duplication of a game program per se and the operation thereof according to this invention will be explained in detail in conjunction with the foregoing description.

Referring to Figure 3 through 5 there are shown by way of typical embodiments of the invention circuit diagram of the logic elements adapted to control the external information.

In each case of such typical embodiments of this invention, these logic elements are arranged releasably or interchangeably in the game machine circuit like the external memory 16 stated above. With the addition of such elements, when a player who desires to play on a new or different game program feeds this program into the game machine by operating the external memory, this external information is to be controlled preliminarily under a certain state, or alternatively is stored once in the internal program memory 37 so as to be controlled and read out thereafter. As a consequence, the external information would not b made available in effect only with such an external operation, and therefore, the game machine does not operate accordingly. For this reason, there is provided such an advantageous feature of the invention that any knowhow to create a new program effectively be protected from being improperly appropriate or duplicated by a third party, despite its interchange ability of a game content.

More specifically, the means to prevent an improper duplication of a game program is now to be described in more detail by way of preferred embodiments of the invention.

Referring now to Figure 3, there are shown the logic elements 60 inserted in such a manner that when having eight-bit data, e.g., (1, 0, 1, 1, 0, 0, 1, 0) stored in the internal memory 37, data with a part thereof (two bits in the first) altered, i.e., (0, 1, 1, 1, 0, 0, 1, 0) is initially stored at the external memory 16, thereafter that changed part being decoded in the circuit comprising the logic elements 60. That is, according to the arrangement of elements 60, it is arranged that even if one bit line D_1 among the output lines at the control 40 of the external memory is switched interchangedly with a second line D_2, all other bit lines D_3 through D_8 are each left unchanged in connection to one of the inputs of AND gates 60*a* through 60*h*. Therefore, a control signal generated in synchronization with a current timing to enable the setting of a modified information from externally may be suitably be fed to the unconnected or open input of that AND gate from a CPU 22.

Now, with respect to the embodiment shown in Figure 4, there are inserted an array of elements 70 which correspond to the logic elements 60 stated above. As reviewed hereinbefore, since a new external information created due to a current desire of a game player to change a code is now stored into the internal program memory 37 through the control 40 and the interface 41, the program content in the memory 37 is now decoded by a CPU 22 at the time a CPU 22 reads out this program content, and thus is formed in an information to be effected in the game machine circuit.

In other words, as the array of logic elements 70 comprises above mentioned AND gates 70a through 70h which are inserted from the data bus section (DB_1 through DB_8) to the input/output terminal (PD_1 through PD_8) of the program memory 37, the AND gates open with the control signal from a CPU 22 and thus having the new external information stored at the above mentioned memory 37, and on the other hand, according to the arrangement of element 70, it is arranged that when a control signal is sent out of a CPU 22, the outputs of the first and second input/output terminals PD_1 and PD_2 are connected interchangedly with each other, while all other outputs (those from the remaining input/output terminals PD_3 through PD_8) are to be sent to above mentioned data bus section DB_1 through DB_8 as they are.

Next, a fourth embodiment of this invention will be described in conjunction with Figure 5 wherein there is inserted an array of logic elements 80 shown in Figure 1. In order that a new external information is set, a certain value is stored preliminarily in the array of elements 80. Only when a value of data introduced in each predetermined time of a game and the value stored at above elements 80 are found to be identical, an arbitrary number, for instance, 1 is added to that value stored, and then th resultant value is read out at each predetermined time.

In the case that there is found any difference between above mentioned value of data and the value in the elements 80, the new external information is held inactive at the control 40. Or alternatively, it may be arranged such that the array of elements 80 operates after the storage of that information at the program memory 37. More specifically, since the array of logic el ments 80 comprises a counter 80*p* (see Figure 5) which is adapted to preset the external information in the parallel fashion, the element operates to preset in accordance with the first control signal from a CPU 22, and consequently, upon the receipt of the output from a pulse generating circuit 80*q* at a clock terminal CK, the counter 80*p* functions to count up the preset content by each increment value of 1. And at the same time, thus-counted-up output is sent to the input of one of the AND gates 80*a* through 80*h*. In this manner, the control signal is delivered when the external information is read out and for instance, at each 128 bytes.

On other hand, since a second control signal is fed to the input terminals of the AND gates that did not receive such count-up with a small time delay from the initial (first) signal, that AND gate now delivers the output from the counter 80*p* to the data bus section (DB_1 through DB_8). At this stage, the outputs are checked by a CPU 22 for any abnormality in the external information taken.

CLAIMS

1. A video game machine for electronically displaying a game content on a screen of a video monitor including a microprocessor for controlling transfer of information relating to a game program from an operating memory to a program memory, the arrangement being such that the operating memory is adapted to be interchangeable with one or more of the said operating memory or memories.

2. A video game machine for electronically displaying a game content on a monitor screen;
wherein an external information relating to a game program to be transferred from an operating memory external of said game machine into an internal program memory is arranged to be controlled by a microprocessor;
and wherein said external control memory is arranged to be interchangeable with another.

3. The video game machine as claimed in claim 1 or claim 2;
wherein said microprocessor is adapted to access a boot-strap memory and read out an external information upon the receipt of the output from a reset circuit and wherein said microprocessor is further adapted to read said external information even when a current game being played is interrupted.

4. The video game machine as claimed in any one of the preceding claims further comprising an array of of control logic elements for controlling an external information connectable in combination to said internal program memory; and
wherein the circuit including said array of logic elements is adapted to operate in such a manner that only a desired one of said external information may be transferred into said program memory under the control of said microprocessor, or in such a manner

that said desired information stored in said program memory may be recontrolled in modification once again; and

wherein said array of logic elements is arranged to be detachable from said circuit of logic elements.

5. A video game machine for electronically displaying a game content on monitor screen substantially as hereinbefore described with reference to the accompanying drawings.

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